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Optimized 0.1 μm GaAs MESFET's

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Abstract

We have optimized the design of conventional GaAs MESFET's for high frequency operation. FET's were fabricated using electron beam lithography to define 0.1 μm "mushroom" and "Γ" gates. The best results obtained include peak transconductance of 600mS/mm, f_t = 93 GHz, and $f_{max} \geq 150$ GHz. In addition, studies were carried out to examine the effect of gate shape and location on high frequency device performance.

1 Introduction

Although very high f_t's have been demonstrated for GaAs MESFET's[1] [2] [3], f_{max}'s high enough to be competitive with other millimeter-wave devices such as high-performance MODFET's have not been demonstrated. The purpose of this work is to show that with a well controlled process and careful device design, conventional GaAs FET's can have excellent DC and high frequency performance, including high transconductance, high f_t, and high f_{max}. The effect of gate shape and location on frequency performance has also been studied. f_{max}'s as high as 150 GHz have been realized, showing that GaAs MESFET's are competitive devices for some millimeter-wave applications. This is among the highest f_{max} values reported for a GaAs MESFET.

2 Fabrication

GaAs MESFET's were fabricated on thin, highly doped, n-type MBE epi-layers. The ohmic cap was doped as high as possible to reduce extrinsic channel resistance, while the active layer doping was designed to be high enough to minimize short channel effects but low enough to fabricate a good Schottky barrier and have reasonably low gate capacitance. The layer design is shown in Figure 1. The device fabrication started with mesas, which were defined using an AZ-5214 positive process and etched to a depth of approximately 3000Åusing a 3:1:50 $H_3PO_4 : H_2O_2 : H_2O$ mixture. Next, n-type ohmic contacts with both 2 and 3 micron source-drain spacings were defined using an AZ-5214 image reversal liftoff process. Ni/Ge/Au/Ti/Au ohmic metal was deposited using an electron-beam evaporation system, and the ohmics were annealed on hotplates. Ohmic contact resistance was measured using the TLM technique to be $4x10^{-7}\Omega - cm^2$

Nominally 0.1 μm gates were defined using a bi-layer resist electron-beam lithography liftoff process. Both "T"-shaped and "Γ"-shaped gates were defined using three beam scans consisting of one footprint and two sidelobe scans. The sidelobes were on either side of the footprint for the "T" gates and at two different points on the same side of the footprint for the "Γ" gates. An aspect ratio of approximately 3:1 was achieved for both gate structures. Channels were recessed using either 11:1:44 $Citric\ acid : H_2O_2 : H_2O$ or 1:1:60 $H_3PO_4 : H_2O_2 : H_2O$. Ti/Pt/Au gates were metallized in an electron-beam evaporation system. For both gate shapes, three different gate-source spacings were used, in order to examine the effect of gate-source spacing on high frequency device performance. Gates were placed first in the center of the source-drain gap, and then moved towards the source by 0.25 μm and 0.5 μm for the 2 μm source-drain gap, or 0.5 μm and 1.0 μm for the 3 μm source-drain gap. Figure 2 shows SEM photographs of the MESFET gate cross-sections.

Layer	Thickness
n+ GaAs ohmic cap n=5e18	40 nm
n GaAs channel n=2.5e18	65 nm
Undoped GaAs buffer	1 µm
Undoped superlattice buffer	
Semi-insulating GaAs substrate	

Figure 1: Layer structure for 0.1 μm GaAs MESFET

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3 Results

Several devices were tested for both "T" and "Γ" gate shapes and the three different gate-source spacings to examine the effect of gate shape and gate-source spacing on device performance. The data presented for statistical comparison comes from a sample of approximately 75 MESFET's, and the numbers presented represent real average values for the process, not just peak performance.

DC device characterization was done using an HP-4145B semiconductor parameter analyzer. The citric acid recessed FET's showed I_{DSS} varying from 51.0 mA to 80.2 mA and transconductances varying from 328 mS/mm to 480 mS/mm for 100 μm wide gates in a "Π" configuration. The phosphoric acid recessed FET's had a greater range of saturation currents and transconductances, with I_{DSS} ranging from 10.4 mA to 55.5 mA and transconductances varying from 357 mS/mm to 592 mS/mm for 100 μm wide gates in either "T" or "Π" configurations.

On-wafer RF characterization was done over a wide range of DC bias conditions, from 0.5 GHz to 24.0 GHz using a Cascade Microtech probe station and an HP-8510B network analyzer. For all frequency extrapolations, a 6 dB per octave roll-off was assumed for both f_t and f_{max}. This should give accurate f_t and conservative f_{max} values. All extrapolations were taken directly from S-parameter data without any use of equivalent circuits. K values were less than one and the slope of GMAX was still 3 dB per octave for all the peak f_{max} numbers presented.

For the citric acid recess, f_t values ranged from 68.9 GHz for the "Γ" shaped gates set closest to the source in a 2 μm source-drain gap, to 85.8 GHz for the "mushroom" shaped gate with the middle gate-source spacing in a 2 μm source-drain gap, when averaged over devices in the respective configurations. f_{max} ranged from 98.9 GHz for the "Γ" gates centered in a 3 μm source-drain gap to 116.1 GHz for the "mushroom" gates moved 1.0 μm toward the source in a 3 μm source-drain gap. These values are all for gates in a Π-configuration.

For the phosphoric acid recess, average f_t's varied from 60.4 GHz for the "mushroom" gate in a Π configuration moved closest to the source in a 2 μm source-drain gap to 88.6 GHz for the "Γ" gate in a T-configuration centered in a 2 μm source-drain gap. The f_{max} values ranged from 113.5 GHz for the "mushroom" gate in a Π configuration closest to the source in a 2 μm source-drain gap to 135.2 GHz for the "mushroom" gate in a T configuration with the middle spacing in a 2 μm source-drain gap.

In a different gate write with a slightly lower dose, and, thus, slightly smaller gate length, excellent MESFET device performance was observed. The gate was recessed with the phosphoric acid mixture. DC results for several transistors showed transconductances varying from a minimum of 490 mS/mm to a maximum of 600 mS/mm. High frequency results showed f_t varying from 83 GHz to a high of 93 GHz and f_{max} varying from 122 GHz to over 150 GHz (GMAX = 16 dB at 24 GHz with K = 0.9). DC and high frequency results

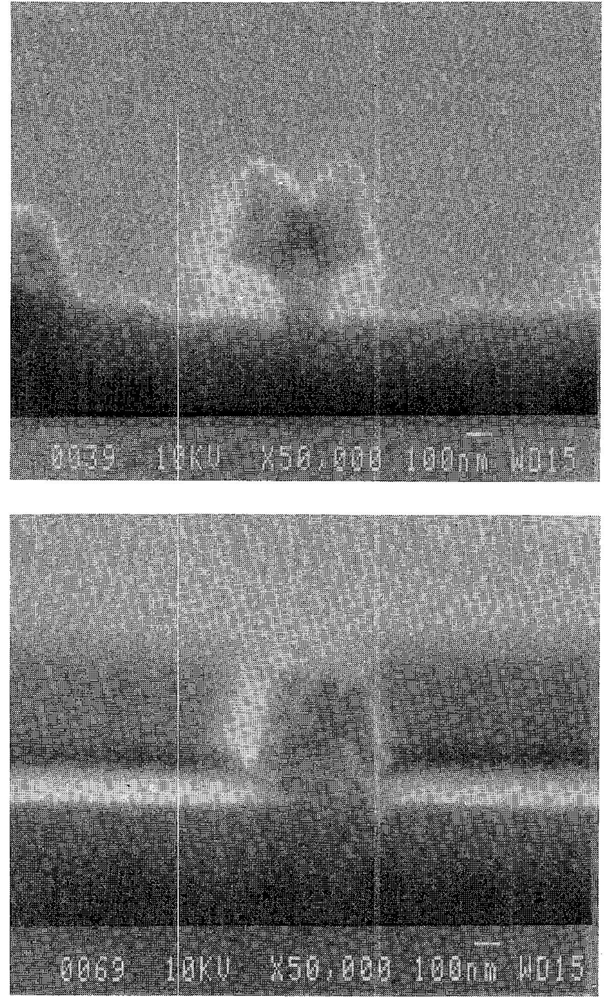

Figure 2: SEM cross-section of nominally 0.1 μm gate GaAs MESFET's. Top is "T"-shaped and bottom is "Γ"-shaped.

for the best of these devices can be seen in Figures 3, 4, and 5.

4 Discussion

The effects of gate-source spacing on frequency performance can be fairly easily explained through simple models for f_t and f_{max}. In a first order approximation, f_t can be expressed as: [4]

$$f_t = \frac{v_{sat}}{2\pi L} = \frac{g_m}{2\pi C_{gs}} \quad (1)$$

f_{max}, to a first order, is: [4]

$$f_{max} = \frac{f_t}{2\sqrt{\frac{R_s+r_i+R_g}{r_d} + 2\pi f_t R_g C_{gd}}} \quad (2)$$

where v_{sat} is the electron saturation velocity, L is the gate length, g_m is the FET extrinsic transconductance, C_{gs} is the

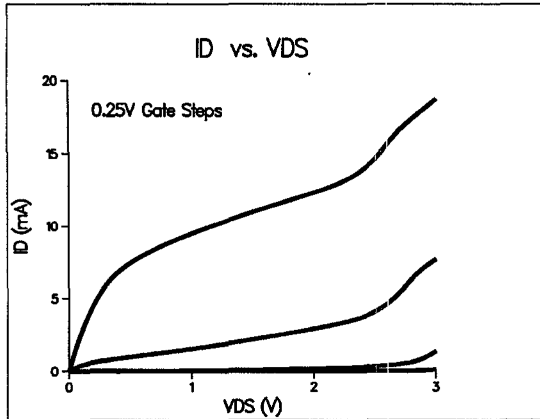

Figure 3: DC $I_D - V_{DS}$ characteristics for $0.1\mu m$ GaAs MESFET

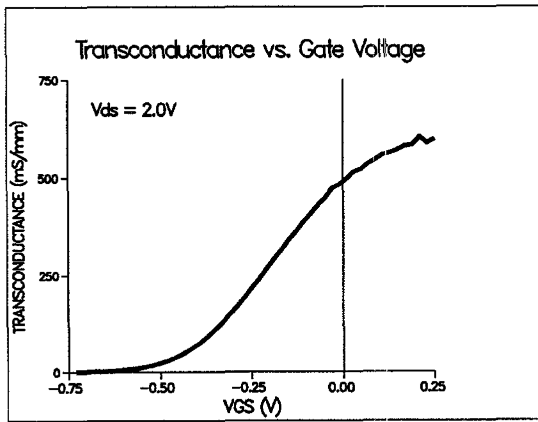

Figure 4: DC $g_m - V_{GS}$ characteristics for $0.1\mu m$ GaAs MESFET

gate-to-source capacitance, R_g is the gate resistance, r_i is the intrinsic FET input resistance, R_s is the parasitic source resistance, r_d is the FET output resistance, and C_{gd} is the gate-to-drain capacitance.

As the gate is moved closer to the source, three major effects should occur: 1) R_s will decrease, causing an increase in the extrinsic transconductance, g_m, 2) the fringing/metal-to-metal portion of C_{gs} will increase, and 3) the fringing portion of C_{gd} will decrease. As the gate moves toward the source, if the decrease in R_s and the increase in g_m are not as great as the increase in the fringing portion of C_{gs}, f_t will drop. On the other hand, a decrease in both R_s and C_{gd} will increase f_{max} as the gate moves towards the source. Despite some variation in transconductances, these effects can be seen in the different gate configurations and recesses.

For the citric acid recess and the "mushroom" gates, f_t starts at an intermediate value, peaks for the gate slightly offset towards the source, and then has its minimum for the gate closest to the source for both the 2 and the 3 micron source-drain gaps. First, f_t improves as the gate is moved slightly towards the source causing a decrease in R_s and an increase in g_m. However, as the gate is moved even closer

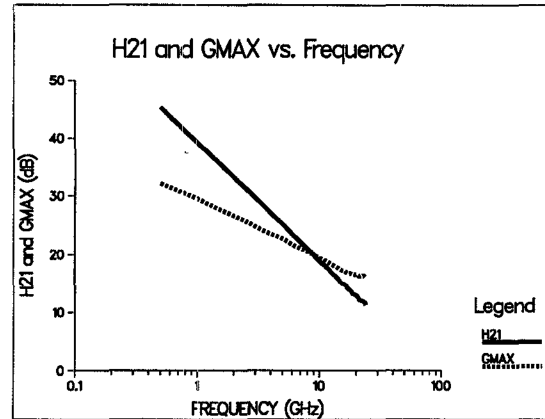

Figure 5: High frequency results for 0.1 μm GaAs MESFET

to the source, the increase in C_{gs} becomes too great and f_t falls off again. f_{max} shows the opposite trend, generally exhibiting a monotonic increase as the gate is moved closer to the source. This shows the significance of the decrease in both R_s and C_{gd}, particularly since f_{max} is able to increase while f_t, a linear term in f_{max}, decreases.

A comparison of results for "mushroom" and "Γ" gate shapes for the citric recess provides additonal insight into the parasitics of the different gate shapes. For the "Γ" gates, the average transconductances are lower than those of the "mushroom" gates, but the f_t values are similar. This illustrates that the fringing portion of C_{gs} is smaller for the "Γ" gates, which is logical since there is minimal metal overhang on the source side of the "Γ" gate. On the other hand, the f_{max} values are lower for the "Γ" gates than for the "mushroom" gates. Since transconductance is already factored out by the f_t term in the numerator of f_{max}, this must reflect an increased parasitic C_{gd} due to the additional metal on the drain side of the gate.

For the citric recess, in every case but one (f_{max} for L_{gs} = $0.45\mu m$, "Γ"), the transconductance, f_t, and f_{max} were lower for the 3 μm than for the 2 μm source-drain gap. This reflects the increased R_s associated with the wider source-drain spacing.

For the phosphoric acid recess, f_t shows a generally monotonic decrease in all cases as it moves closer to the source for both the Π and T configurations. This probably reflects both decreased transconductance and increased C_{gs}. For the Π configuration, since the percentage decreases in f_t's are comparable to the simultaneous decreases in g_m's, the decrease in R_s is probably of about the same impact as the increase in C_{gs}. However, for the T configuration, the decrease in f_t is not as great as the decrease in transconductance. This means that in this case, the impact of R_s is probably greater than that of C_{gs}. The trend of f_{max} for the phosphoric recess is to start at an intermediate value, increase slightly as the gate is moved part-way toward the source, and then to decrease as the gate is moved closest to the source. In general, the decrease in f_{max} is not as much as that of f_t, reflecting the improvements in R_s and C_{gd}.

Gate Geometry	g_m	f_t	f_{max}
$L_{gs} = 0.95\mu m$, mushroom	433	82.5	112.2
$L_{gs} = 0.70\mu m$, mushroom	449	85.8	115.4
$L_{gs} = 0.45\mu m$, mushroom	451	73.3	114.1
$L_{gs} = 0.95\mu m$, gamma	404	82.5	103.3
$L_{gs} = 0.70\mu m$, gamma	404	81.4	104.1
$L_{gs} = 0.45\mu m$, gamma	381	68.9	110.0

Table 1: Results for citric acid recess with 2 μm source-drain gap and "Π" gate configuration

Gate Geometry	g_m	f_t	f_{max}
$L_{gs} = 0.145\mu m$, mushroom	405	76.3	107.0
$L_{gs} = 0.95\mu m$, mushroom	415	80.0	111.3
$L_{gs} = 0.45\mu m$, mushroom	432	74.2	116.1
$L_{gs} = 0.145\mu m$, gamma	382	75.6	98.9
$L_{gs} = 0.95\mu m$, gamma	369	73.4	102.0
$L_{gs} = 0.45\mu m$, gamma	389	71.9	105.2

Table 2: Results for citric acid recess with 3 μm source-drain gap and "Π" gate configuration

Gate Geometry	g_m	f_t	f_{max}
$L_{gs} = 0.95\mu m$, mushroom	456	74.8	120.8
$L_{gs} = 0.70\mu m$, mushroom	469	72.9	125.0
$L_{gs} = 0.45\mu m$, mushroom	398	60.4	113.5
$L_{gs} = 0.95\mu m$, gamma	546	79.7	128.1
$L_{gs} = 0.70\mu m$, gamma	531	80.1	127.8
$L_{gs} = 0.45\mu m$, gamma	490	70.3	116.7

Table 3: Results for phosphoric acid recess with 2 μm source-drain gap and "Π" gate configuration

Gate Geometry	g_m	f_t	f_{max}
$L_{gs} = 0.95\mu m$, mushroom	558	85.7	134.0
$L_{gs} = 0.70\mu m$, mushroom	530	85.2	135.2
$L_{gs} = 0.45\mu m$, mushroom	512	82.6	134.4
$L_{gs} = 0.95\mu m$, gamma	577	88.6	130.6
$L_{gs} = 0.70\mu m$, gamma	593	83.6	132.0
$L_{gs} = 0.45\mu m$, gamma	566	88.6	118.8

Table 4: Results for phosphoric acid recess with 2 μm source-drain gap and "T" gate configuration

A comparison of "mushroom" and "Γ" gates for the phosphoric recess shows generally better performance for the "Γ" gates. This is probably due to higher transconductances for the "Γ" gates. For the "T" configurations, f_{max} is higher for the "mushroom" than the "Γ" gates, demonstrating the increased C_{gd} for the "Γ" shape. The improved performance of the "T" over the "Π" configurations is largely due to increased transconductance. This is probably an artifact of the mask set used, where the probing pads are longer for the "Π" than for the "T" devices, causing the "Π" devices to have a larger parasitic pad resistance.

The differences in the two recess etchants can also be explained through parasitics. The phosphoric recess is a "tighter" recess than the citric recess–the phosphoric etchant has less lateral undercut than the citric. This will mean higher transconductances for the phosphoric recess, since the effective gate length is shorter, but it will also mean larger fringing effects from C_{gs} and C_{gd} for the phosphoric recess since the gate is closer to the ohmic cap. This results in a higher f_t for the citric recess, reflecting the lower C_{gs} for that etchant. f_{max} is higher for the phosphoric etch; this is primarily from the increased transconductance.

The comparison of the gate recesses, shapes, and configurations provides interesting insight into the various parasitics of the different gates. However, probably the most important fact that comes from the data is that changes even of the order of tenths of microns in gate location or shape can make enough difference in source resistance and fringing capacitances to have a significant effect on overall device performance when gate lengths are of the order of 0.1 μm. In general, the study of the effect of gate-source spacing and gate shape on device performance gives two importance pieces of information for device designers. First, it provides information for the device designer to use to minimize parasitic effects in devices. Second, it illustrates that design of a transistor with high f_t is probably quite different from design of a transistor with high f_{max}.

The peak device performance reported in this paper is among the best reported to date for GaAs MESFET's. The DC extrinsic transconductance of 600 mS/mm is comparable to the best values seen in the literature for devices with conventional layer structures, and the f_{max} of 150 GHz is the highest reported to date. This excellent device performance shows that, with a reliable process and careful device design, conventional GaAs MESFET's can still be competitive as mm-wave devices. In addition, the overall average values for the MESFET's fabricated, particularly for the T configuration devices with the phosphoric recess, are very good.

5 Conclusions

We have shown state-of-the-art performance for conventional GaAs MESFET's built using a well characterized, carefully controlled process. Results include what we believe to be the highest f_{max} reported for a GaAs MESFET. In addition, overall average device performance presented is very good. We have demonstrated a reliable process in which incremental changes can be made, characterized, and implemented in device design. An analysis of device parasitics has been performed which should provide helpful information for design of very high performance GaAs MESFET's that can be used as competitive millimeter-wave devices.

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